REMARKS

Claims 1-14, 16-29 and 31-52 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Teranishi et al. (USPN 6,117,183) (hereinafter referred to simply as "Teranishi"). Furthermore, Claims 15 and 30 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Teranishi in view of McKaskle et al. (USPN 5,481,741) (hereinafter referred to simply as "McKaskle"). Applicant respectfully traverses these rejections based on the following reasoning.

The claimed inventions are related to the field of graphical programming. In graphical programming, a user builds a graphical program by selecting and interconnecting nodes and icons. The resulting diagram may be submitted for execution on a computer system.

Teranishi discloses an interactive CAD apparatus for logic circuit packaging design. Figure 7 of Teranishi illustrates a set of logic components and paths between the components in a tentative circuit design. However, the illustrated logic components and paths between components cannot be interpreted as being part of a graphical program. There is no sense in which the illustrated logic components and paths visually indicate functionality of a graphical program as recited in each of the independent Claims. Instead, the illustrated logic components and paths merely represent a geometrical arrangement of logic components and paths in a proposed circuit design.

Therefore, Claims 10, 18, 26, 32 and 39 and their dependents are patentably distinguished over the cited references.

Furthermore, Teranishi never suggests *propagating information from a first hardware device node to a second hardware device node, where the information specifies the hardware device with which the first hardware device node is associated* as recited in Claims 1, 18 and 32. Indeed, because Teranishi never discloses a graphical program, or, nodes in a graphical program, it is not conceivable that he could teach the propagation of information between nodes of a graphical program. Therefore, Claims 1, 18 and 32, and their dependents, are additionally distinguished over the cited references.

Moreover, Teranishi never suggests any of the following features recited in Claims 10, 26 and 39:

"associating the first hardware device node with a first hardware device class in response to user input";

"selecting a method or property of the first hardware device class for the first hardware device node in response to user input";

"changing the first hardware device node to have an association with a second hardware device class in response to user input"; and

"performing type checking to determine whether the method or property is valid for the second hardware device class, in response to said changing the first hardware device node to have an association with the second hardware device class".

The notion of hardware device class is entirely missing from Teranishi. Thus, it is not possible reasonably construe Teranishi as teaching the operation of associating a hardware device node with a hardware device class, or, the operation of selecting a method or property of a hardware device class as recited in Claims 10, 26 and 39. Therefore, Claims 10, 26 and 39, and their dependents are additionally distinguished over the cited references.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-52100/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,

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